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# Wafer-scale photolithography of ultra-sensitive nanocantilever force sensors

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The detection of small forces using singly clamped cantilevers is a fundamental feature in ultrasensitive versions of scanning probe force microscopy. In these technologies, silicon-based nanomechanical devices continue to be the most widespread high-performance nanomechanical sensors for their availability, ease of fabrication, inherently low mechanical dissipation, and good control of surface-induced mechanical dissipation. Here, we develop a robust method to batch fabricate extreme-aspect-ratio ($10^3$), singly clamped scanning nanowire mechanical resonators from plain bulk silicon wafers using standard photolithography. We discuss the superior performance and additional versatility of the approach beyond what can be achieved using the established silicon on insulator technology.  https://doi.org/10.1063/1.5043479

Suspended nanostructures are at the core of several technologies that sense matter and fields.[1–10] On the one hand, the suspension exposes more sensor surface area to maximize signal from interaction with the analytes and to decrease noise from the substrate.[11] The process simultaneously unleashes mechanical vibration modes, enabling the monitoring of changes in masses and interaction forces through the mechanical frequencies.[12,13] In the past two decades, researchers have pushed the sensitivity performance of various such technologies to levels at and beyond those of single particles,[14] molecules,[15] atoms,[16–18] and spins.[19]

The rapid success, in the laboratory, of many of these new techniques contrasts with their delayed translation into generally adopted research tools and products. A common barrier responsible for the slow popularization, regardless of the physics underlying their operation, is an intrinsic difficulty in mass-producing nanostructured sensors cheaply, with reliable quality, and in serviceable yields. Electron-beam lithography (EBL), serially expensive, is often necessary in top-down fabrications of nanostructured sensors. Post-synthesis, directed assembly of bottom-up nanomaterials, intricately finicky, is unavoidable in the wafer-scale production of derivative sensors.[20–22] As a result, advances in processing techniques that address these technical aspects appear to be a prerequisite to help not only bringing promising emerging technologies towards widespread application, but also advancing the techniques themselves by eliminating one of the bottle-necks hindering experimental progress.

In this letter, we report the wafer-scale photolithography of state-of-the-art ultrasensitive silicon nanocantilevers using inexpensive and readily accessible bulk wafer materials. We combine several silicon micro processing techniques to this end. We achieve resonator widths down to 200 nm by oxidative HF trimming.[23–25] A full release from the substrate is critical for scanning probe applications. We cleave the patterned cantilever structures from the underlying bulk wafer by a fast anisotropic wet etching step,[26,27] after having completely removed the underlying wafer in two separate deep reactive ion etching (DRIE) steps, one from the front and one from the back side.[28] Device lengths in the 100–200 $\mu$m range and thicknesses in the 100–200 nm range ensure superior force sensitivities.[28,29]

While the production of comparable force sensors was demonstrated recently through a combination of silicon on insulator (SOI) and EBL,[30] the present process is faster, more controllable, and improves wafer-scale thickness uniformity at much reduced cost. The processes and sensors reported here therefore have attributes that poise them to become future standards for several ultrasensitive scanning force probe techniques, including magnetic resonance force microscopy (MRFM),[19,29,31–33] magnetic susceptibility force microscopy ($\chi$FM),[34] and vectorial mapping of fields.[9,10]

The devices were batch-fabricated using intrinsic ⟨111⟩-orientated, single-side-polished single crystalline silicon wafers 375 ± 15 $\mu$m in thickness. The fabrication process is schematically illustrated in Fig. 1. To completely remove the bulk wafer material from underneath patterned cantilever beams, the approach incorporates a front-side deep reactive ion etching (DRIE) step with anisotropic wet etching[26] to achieve an etch-stop effect equivalent to that afforded by a hetero-material layer, such as silicon dioxide.[28]

The fabrication starts with a front-side photolithography and inductively coupled plasma (ICP) etching step to define the cantilever patterns [Figs. 1(a) and 1(b)]. The depth of the ICP etch (250 nm here) sets an uniform upper bound on the thickness of the resulting devices. This method offers improved controllability compared to the traditional approach based on SOI; the thinning of the device layer silicon down to the required cantilever thickness in SOI-based processes is delicate with uniformity limited by two factors. A first factor is the specification of the commercial material; typical SOI device layer thickness variations are in the hundreds of nanometers. The second factor is additional variability introduced during thinning from an initially much thicker device-layer (typically 2 $\mu$m for high-quality intrinsic material). This results from temperature non-uniformity and turbulence

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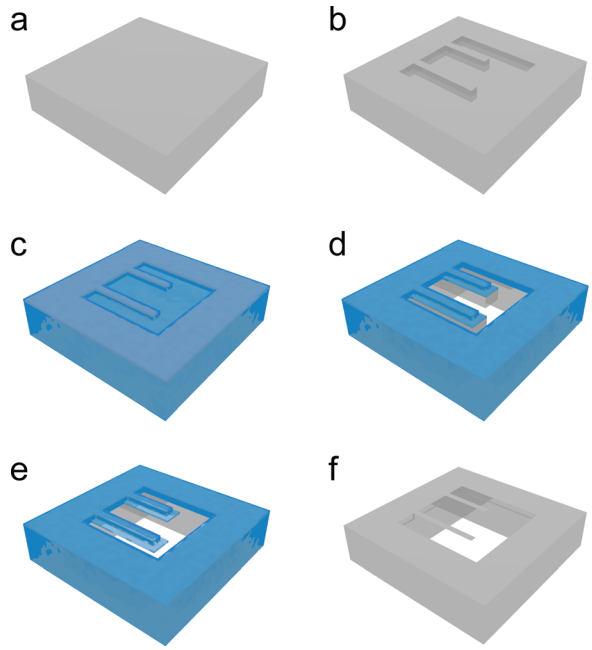


FIG. 1. Schematic summary of the photolithographic fabrication of scanning silicon nanocantilevers. (a) Plain single-crystal silicon ⟨111⟩ wafer. (b) Inductively coupled plasma etching of silicon to define the cantilevers following photolithography. (c) High-temperature (1100 °C) thermal dry-oxidation of silicon for growing a conformal $SiO_2$ layer. (d) Front-side photolithography and deep reactive ion etching of silicon to a depth of $100 \pm 10\,\mu$m, followed by backside DRIE to remove the remaining silicon wafer underneath the sensors. (e) KOH etching of silicon was performed to remove silicon and prerelease the cantilevers. The $SiO_2$ layer is used as hard mask during the orientation-selective wet etching. (f) Final releasing of the silicon cantilevers in hydrofluoric acid solution (48%) by removing the $SiO_2$.

during liquid phase etching, or plasma non-uniformity when using dry etching.[30,35]

In contrast, setting the cantilever thickness from a common reference surface (wafer surface) in a single ICP etching step is more controllable. ICP etch rate variability over a wafer is on the order of 5%. We measured a typical peak-to-peak thickness variation of 15 nm for an etch depth of 250 nm on a 4 in. wafer. This level of variation is competitive with the best SOI wafer specifications that can be sourced (e.g., SOITEC: 1500 nm ± 10 nm).

A conformal thermal oxide layer ($188 \pm 6$ nm) is subsequently grown on the patterned wafer to serve two purposes [Fig. 1(c)]. A primary use of the thermal oxide is as a hardmask to protect the cantilever pattern during substrate removal steps involving both dry and wet etching conditions [Figs. 1(d) and 1(e)]. A concurrent function of the oxidation step is to reduce the photolithographically patterned, width dimension of the cantilever beam.

A second photolithography was performed on the front side to remove the hardmask from areas around the cantilever patterns. Deep reactive ion etching (DRIE) of the front side was performed ($100\,\mu$m) to provide a buffer layer against etch non-uniformity when performing DRIE chip dicing from the backside [Fig. 1(d)]. When most of the wafer material has been removed in the two DRIE steps, the remaining substrate beneath the cantilevers (with thickness defined by the front-side DRIE) was removed by KOH etching [Figs. 1(d) and 1(e)]. Finally, the cantilevers were fully released by etching in hydrofluoric acid [Fig. 1(f)].

Figure 2 shows a scanning electron micrograph (SEM) of a cantilever chip on a wafer. Uniform SEM contrast is consistent with the fact that everything is part of the same single crystal. Features from the front-side and backside DRIE etching steps are clearly visible, respectively, as the outer rectangular frame and the inner, more intricately patterned frame that hugs the chip, protecting the protruding nanocantilevers during chip lift-out.

Figure 3 provides zoom-in views of typical devices. Nanocantilevers have widths between 0.2 and 1.4 $\mu$m and thicknesses below 200 nm [Figs. 3(a)–3(c)]. The width can be further reduced to the same dimensions as the thickness through a combination of pattern reduction and further oxidation [Fig. 3(d)]. The edge smoothness of the device suggests that further width reduction to below 100 nm should be possible. In such nanowire force sensors with aspect-ratio (width over thickness) close to 1, the horizontal and vertical vibration modes would generally display comparable frequencies and sensitivities, permitting simultaneous, 2-dimensional vectorial mapping of forces.[9,10,29]

Figures 4(a) and 4(b) provide a characterization, by atomic force microscopy, of the backside of a nanocantilever placed on a flat silicon reference surface. The measurement reveals that the bottom, KOH-etched surface is smooth with surface roughness on the order of 10 nm. We find a slight lateral sloping of the bottom surface, which is caused by a lateral misalignment of the masking layer with respect to the cantilever features [Fig. 1(d)]. This misalignment leads to one side of the cantilever being released from the underlying bulk silicon earlier, causing this side to be etched by KOH for a slightly longer time. The data suggest that under these conditions, the etch selectivity between {110} and {111} planes is about 30:1.

Figures 4(c) and 4(d) provide mechanical characterization of a device at room temperature by fiber-optic interferometry at a pressure of $4 \times 10^{-5}$ Torr. The mechanical frequency (19.308 kHz) is consistent with a device thickness of 210 nm. The mechanical quality factor ($Q = 24,300$) is comparable to those of SOI-derived devices with a similar geometry.[36]

Top-down fabrication of silicon nanowires in the 0.1–1 mm length range from SOI wafers is an important technological capability.[37] Extending the technique to bulk wafers, as demonstrated here with critical features defined in a single photolithographic step, have additional advantages

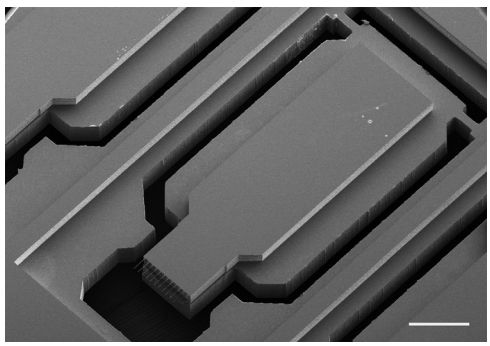

FIG. 2. Representative scanning electron micrograph (SEM) of a device chip, still anchored to the wafer. The device consists of fully suspended nanocantilevers at the tip (bottom left). The chip is supported by two silicon beams at the base (upper right). The scale bar is 0.5 mm.

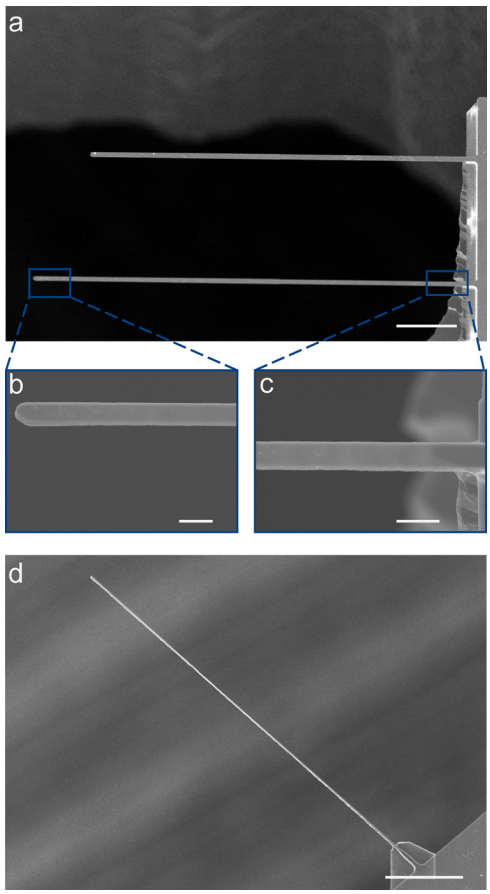


FIG. 3. Suspended singly clamped nanocantilever devices monolithically integrated on chip. (a) Sideview SEM images of nanocantilevers. The bottom-left inset (b) shows the tip of a cantilever and the bottom-right inset (c) show the base of the cantilever. (d) A nanowire cantilever with 200 nm width. The scale bars are 20 $\mu$m (a), 1 $\mu$m (b) and (c), and 10 $\mu$m (d).

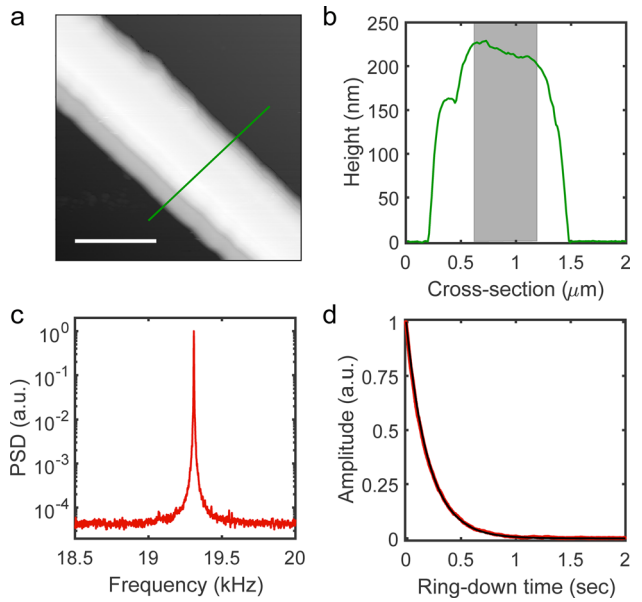


FIG. 4. Characterization of nanocantilever devices. (a) Atomic force micrograph (AFM) of the bottom surface of a typical cantilever. The cantilever was broken off of the chip and positioned, top-face down, onto a flat silicon surface by optical micromanipulation. Green line indicates the location of the profile shown in (b). Scale bar is 1 $\mu$m. (b) AFM profile at the location indicated by the green line in (a). Gray bar indicates the actual width of the cantilever. The wider profile is due to convolution with the AFM tip. (c) Power spectral density (PSD) of a nanocantilever (width = 1.4 $\mu$m, thickness = 210 nm, and length = 120 $\mu$m). (d) Ring-down curve of the same device as in (c).

over bottom-up counterparts. The advantages are both scientific and practical. The greater achievable lengths translate into higher force sensitivity.[4] The precise material composition of readily available commercial bulk wafers would further more enable a quantitative study of the effect of dopant type and doping levels on the mechanical dissipation of silicon. Such a study might potentially lead to better force sensitivities.[38] All of these are difficult to achieve using bottom-up nanowires. In particular, unintentional doping of silicon nanowires by the catalyst particle during vapor-liquid-solid (VLS) growth is a well-studied phenomenon.[29]

From a practical point of view, the deterministic placement of nanowires on the cantilever chip simplifies sample preparation and laser alignment. This will be especially important in future applications of ultrasensitive force microscopies as mature technologies. Nanocantilevers made by the present method have most of their surface area consisting of Si{111}. This orientation is favorable for achieving higher mechanical sensitivity in applications; the corresponding oxide-free surface is more stable in air following chemical passivation, which positively correlates with mechanical sensitivity.[36,39]

Looking ahead, the photolithographic, wafer-scale fabrication of nanocantilevers described here will enable unique opportunities in the research and applications of ultrasensitive force microscopies. Application areas include the detection of single nuclear spins and high-resolution vectorial mapping of fields.[9,10,30,33] The technique will also lead to new types of silicon electromechanical devices, most notably more complex 3-dimensional structures that are not accessible using SOI technology.

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